AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "CROSS-REFERENCE TO RELATED APPLICATIONS" in its entirety and substitute the following section therefor:

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application Serial No. 60/530323, filed on 12/17/2003, which is herein incorporated by reference for all intents and purposes.

[0002] This application is related to the following co-pending U.S. Patent Application, which is filed on the same day as this application, which has a common assignee and at least one common inventor, and which is herein incorporated by reference in its entirety for all intents and purposes:

SERIAL NUMBER	FILING DATE	TITLE
10/816020 (CNTR.2207)	~~HEREWITH~~04/01/2004	INSTANTANEOUS FREQUENCY-BASED MICROPROCESSOR POWER MANAGEMENT

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0008] A frequency-voltage mechanism for power management according to an embodiment of the present invention includes first and second PLLs, select logic, control logic, and voltage control logic. The first PLL generates a first source clock signal at a first frequency based on a bus clock signal. The second PLL generates a second source clock signal at a second frequency based on a first frequency control signal and the bus clock signal. The second PLL generates a first frequency lock signal when the second source clock signal achieves a reduced frequency indicated by the first frequency control signal. The select logic selects between the first and second source clock signals to provide a core clock signal based on a select signal. The clock control logic detects

power conditions via at least one power sense signal, provides the first frequency control signal according to the power conditions, and provides the select signal. The clock control logic controls the select signal to switch the core clock signal from the first PLL to the second PLL in response to the first frequency lock signal. The voltage control logic adjusts the operating voltage commensurate with frequency of the core clock signal.

[0009] It is appreciated that the frequency-voltage mechanism provides means for dynamically adjusting the power consumed in a manner that does not incur undue delays and that provides power efficiency benefits over stand-alone frequency or voltage modulation techniques. The clock control logic selects one source clock signal while ramping the other, and then switches when the second source clock signal achieves a desired frequency. Switching is effectively instantaneous, such as, for example, within one cycle of the bus clock signal. The first PLL may be implemented as a fixed-frequency device (e.g., at a maximum frequency level) or as a programmable device similar to the second PLL. For example, the first PLL may generate the first clock source signal based on a second frequency control signal and provide a second lock signal indicative thereof. In this case, the clock control logic provides the second frequency control signal and receives the second lock signal.

[0010] In ~~various~~ embodiments~~, the~~ where the second PLL generates a first frequency lock signal when the second source clock signal achieves a reduced frequency indicated by the first frequency control signal~~. In this case,~~, and where the clock control logic switches the core clock signal from the first PLL to the second PLL in response to the first frequency lock signal, the voltage~~. The voltage~~ control logic reduces the operating voltage after the core clock signal is switched. The voltage control logic increases the operating voltage in response to increase power conditions, and then clock control logic switches to the first PLL after the operating voltage is increased. If the first PLL is programmable, then the clock control logic further waits for the second lock signal before switching. In one embodiment, the clock control logic and the voltage control logic cooperate to increase the operating voltage prior to increasing frequency of the core clock signal and to decrease the operating voltage after decreasing frequency of the core clock signal.

[0011] A power supply may be provided that adjusts the operating voltage based on a voltage step signal from the voltage control logic. The power supply provides a voltage lock signal indicative thereof to the clock control logic. Thus, the clock control logic increases frequency of the core clock signal only after the voltage has been increased to the proper level.

[0012] A microprocessor according to an embodiment of the present invention includes a power condition sense interface, an operating voltage interface, first and second PLLs, a clock controller, select logic, and a voltage controller. The power condition sense interface receives at least one power sense signal indicative of power conditions. The first PLL generates a first source signal at a frequency based on a bus clock signal and a first core ratio bus value and provides a corresponding first lock signal. The second PLL generates a second source signal at a frequency based on the bus clock signal. The clock controller provides a select signal for switching between the first and second PLLs, provides the first core ratio bus value to control frequency of the first source signal, and receives the first lock signal. The select logic selects between the first and second PLLs based on the select signal to provide a core clock signal. The voltage controller adjusts operating voltage commensurate with frequency of the core clock signal.

[0013] In various embodiments, the second PLL may be fixed or programmable. The clock controller and the voltage controller cooperate to decrease operating voltage after decreasing frequency of the core clock signal and to increase operating voltage before increasing frequency of the core clock signal.

[0014] A method of frequency-voltage control for microprocessor power management includes generating a first source clock at a first frequency based on a bus clock signal and a first ratio bus value, generating a second source clock at a second frequency based on the bus clock signal and a second ratio bus value, sensing power conditions, switching core operating frequency between the first and second source clock signals based on sensed power conditions, and selecting operating voltage commensurate with the core operating frequency.

[0015] The method may further include initially selecting the first source clock signal, providing the second ratio bus value based on reduced power conditions to indicate a reduced frequency, ramping the second source clock signal to the reduced frequency in response to the second ratio bus value, detecting a first lock indication when the second source clock signal achieves the reduced frequency, switching to the second source clock signal when the lock indication is detected, and reducing operating voltage commensurate with the reduced frequency after said switching. The method may include switching within one bus clock cycle. The method may include sensing increased power conditions, increasing operating voltage commensurate with the sensed power conditions, and switching to the first source clock signal. In this latter case, prior to switching to the first source clock signal, the method may include determining an increased power level appropriate for the increased power conditions, providing the first ratio signal indicative of an increased frequency based on the increased power level, ramping the first source clock signal to the increased frequency, increasing operating voltage commensurate with the increased frequency, and detecting a second lock indication when the first source clock signal achieves the increased frequency.